A Crossbar Device For Reconfigurable Circuit

ABSTRACT OF THE DISCLOSURE

A crossbar device includes a first set of input lines and a second set of output lines. A plurality of chains of pass transistors are provided to selectively couple the input lines to the output lines in a reduced parasitic capacitive loading manner. Further, memory elements and decoder logic are provided to facilitate control of the selective coupling. Additionally, a low power application of multiple crossbar devices to a reconfigurable circuit block is improved by having each memory element of a crossbar device be provided with a supply voltage higher by a Vth to maintain the input voltage of corresponding output buffers at Vdd,. Further, an application of multiple crossbar devices to a reconfigurable circuit block is improved by coupling a control circuitry via a control line to all output buffers of the interconnected crossbar devices to force the output buffers to a known state at power-on.